

ram64\_1.bls

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Module : 'ram64'  
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## Input files:

ABEL PLA file : ram64.tt3  
Device library : P16V8C.dev

## Output files:

Report file : ram64.rep  
Programmer load file : ram64.jed  
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```
ROMDI = ( !NROMDI.PIN
          # !AB34567 & !NIORQ & NM1 & AB2 & AB0 & AB1 );

HRAM = ( !NHRAM.PIN
          # !AB34567 & !NIORQ & NM1 & AB2 & AB0 & !AB1 );

NDIEN = !( ROMDI.PIN & !NRD
            # !AB15 & AB14 & !NRD
            # SCHALT & AB15 & !AB14 & !NRD );

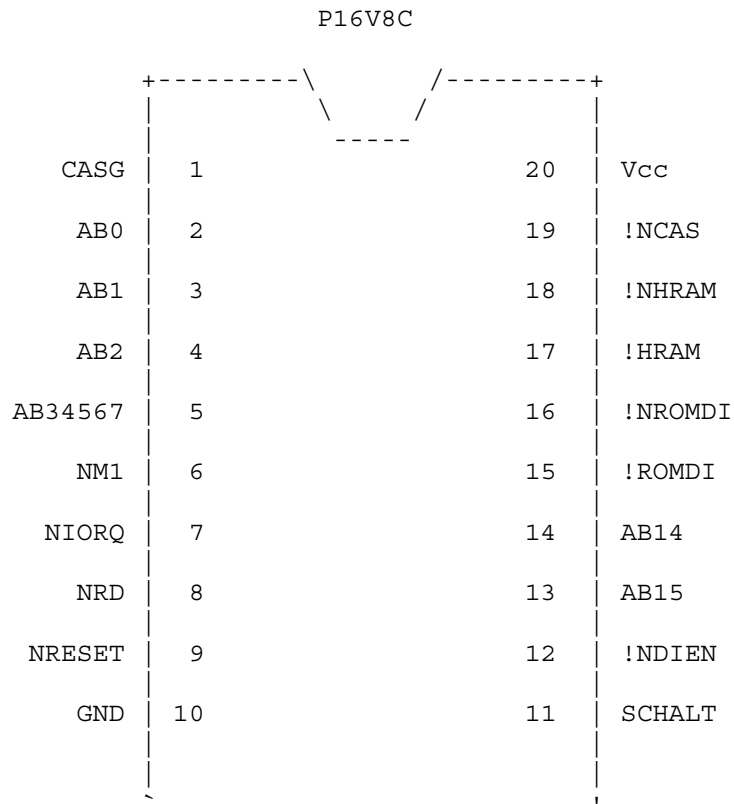
NHRAM = ( !HRAM.PIN
          # !NRESET
          # !AB34567 & !NIORQ & NM1 & AB2 & !AB0 & !AB1 );

NROMDI = ( !ROMDI.PIN
           # !NRESET
           # !AB34567 & !NIORQ & NM1 & AB2 & !AB0 & AB1 );

NCAS = !( CASG );
```

P16V8C Chip Diagram:

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SIGNATURE: N/A

P16V8C Resource Allocations:

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Device Resources	Resource Available	Design Requirement	Unused
<b>Input Pins:</b>			
Input:	10	10	0 ( 0 %)
<b>Output Pins:</b>			
In/Out:	6	6	0 ( 0 %)
Output:	2	2	0 ( 0 %)
<b>Buried Nodes:</b>			
Input Reg:	-	-	-
Pin Reg:	-	-	-
Buried Reg:	-	-	-

P16V8C Product Terms Distribution:

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Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
ROMDI	15	2	7	5
HRAM	17	2	7	5
NDIEN	12	3	7	4
NHRAM	18	3	7	4
NROMDI	16	3	7	4
NCAS	19	1	7	6

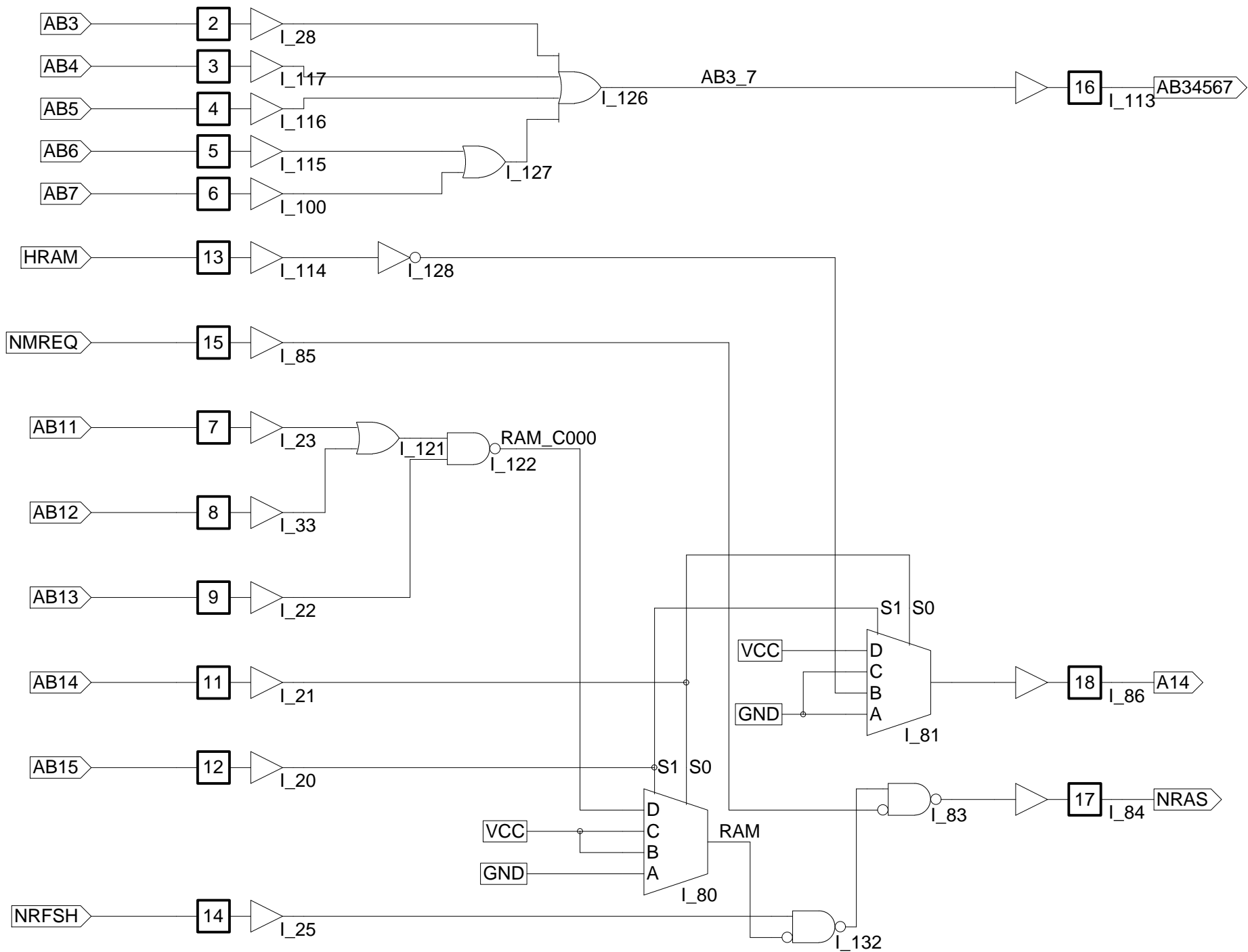
==== List of Inputs/Feedbacks ====

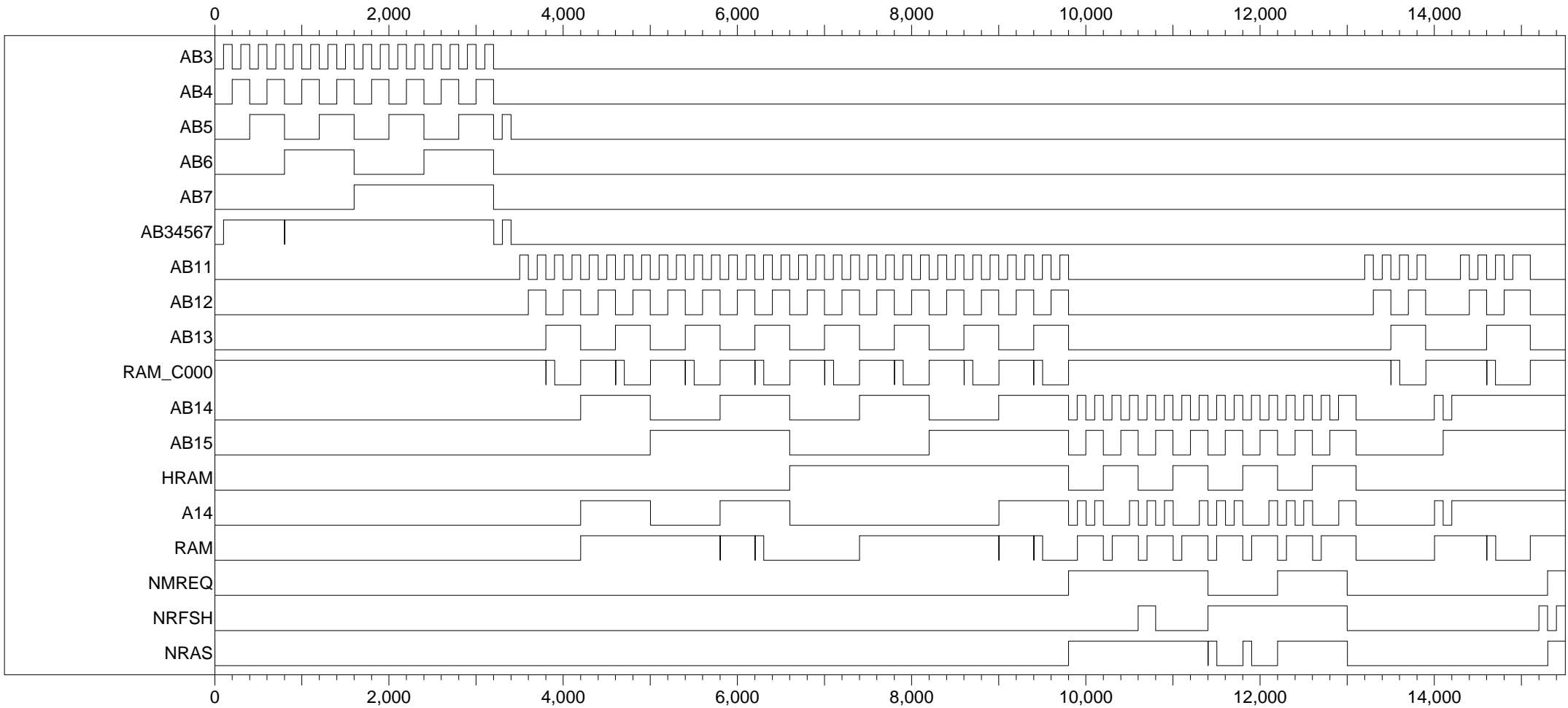
Signal Name	Pin	Pin Type
NROMDI.PIN	16	COMB FB
NHRAM.PIN	18	COMB FB
ROMDI.PIN	15	COMB FB
HRAM.PIN	17	COMB FB
AB34567	5	INPUT
CASG	1	INPUT
SCHALT	11	INPUT
AB15	13	BIDIR
AB14	14	BIDIR
NRD	8	INPUT
NRESET	9	INPUT
NIORQ	7	INPUT
NM1	6	INPUT
AB2	4	INPUT
AB0	2	INPUT
AB1	3	INPUT

P16V8C Unused Resources:

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Pin Number	Pin Type	Product Terms	Flip-flop Type
-	-	-	-





ram64\_2.bls

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Module : 'ram64'  
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Input files:

ABEL PLA file : ram64.tt3  
Device library : P16V8R.dev

Output files:

Report file : ram64.rep  
Programmer load file : ram64.jed  
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P16V8R Programmed Logic:  
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```
NRAS      = (  !AB15 & !AB14 & NRFSH
               #   AB15 & AB14 & AB13 & AB11 & NRFSH
               #   AB15 & AB14 & AB13 & NRFSH & AB12
               #   NMREQ );

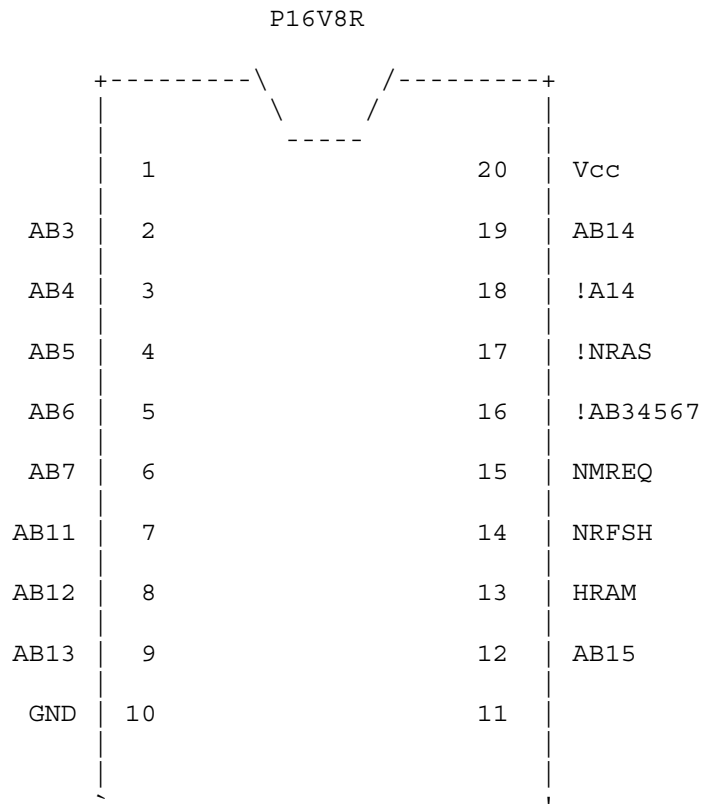
AB34567   = !(  !AB7 & !AB6 & !AB5 & !AB4 & !AB3 );

A14       = !(  HRAM & !AB15
               #   !AB14 );
```



P16V8R Chip Diagram:

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SIGNATURE: N/A

P16V8R Resource Allocations:

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Device Resources	Resource Available	Design Requirement	Unused
<b>Input Pins:</b>			
Input:	10	8	2 ( 20 %)
<b>Output Pins:</b>			
In/Out:	8	8	0 ( 0 %)
Output:	-	-	-
<b>Buried Nodes:</b>			
Input Reg:	-	-	-
Pin Reg:	8	0	8 (100 %)
Buried Reg:	-	-	-

P16V8R Product Terms Distribution:

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Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
NRAS	17	4	7	3
AB34567	16	1	7	6
A14	18	2	7	5

==== List of Inputs/Feedbacks ====

Signal Name	Pin	Pin Type
AB7	6	INPUT
HRAM	13	BIDIR
AB6	5	INPUT
AB5	4	INPUT
AB4	3	INPUT
AB15	12	BIDIR
AB14	19	BIDIR
AB13	9	INPUT
AB11	7	INPUT
NRFSH	14	BIDIR
AB3	2	INPUT
AB12	8	INPUT
NMREQ	15	BIDIR

P16V8R Unused Resources:

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Pin Number	Pin Type	Product Terms	Flip-flop Type
-	-	-	-