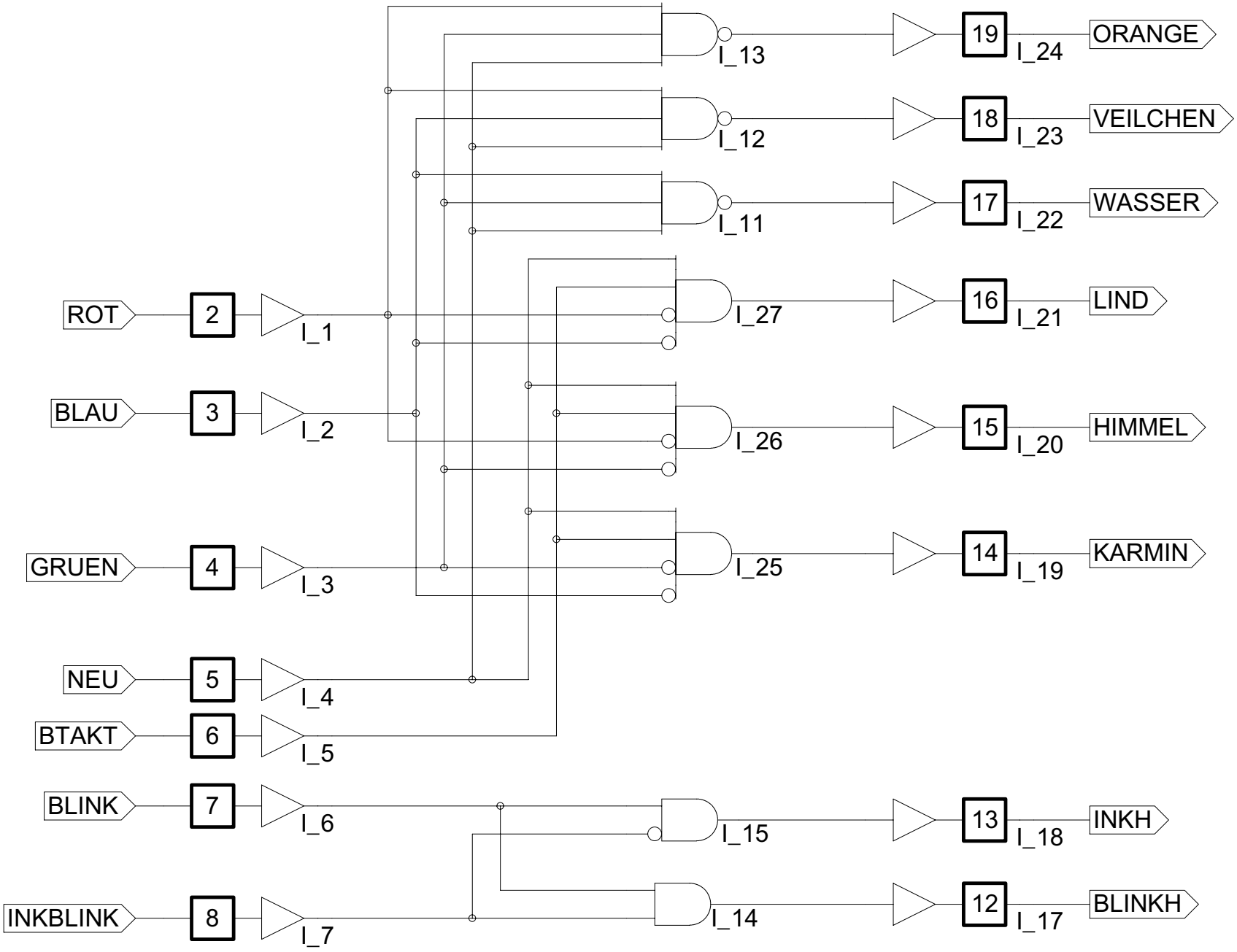
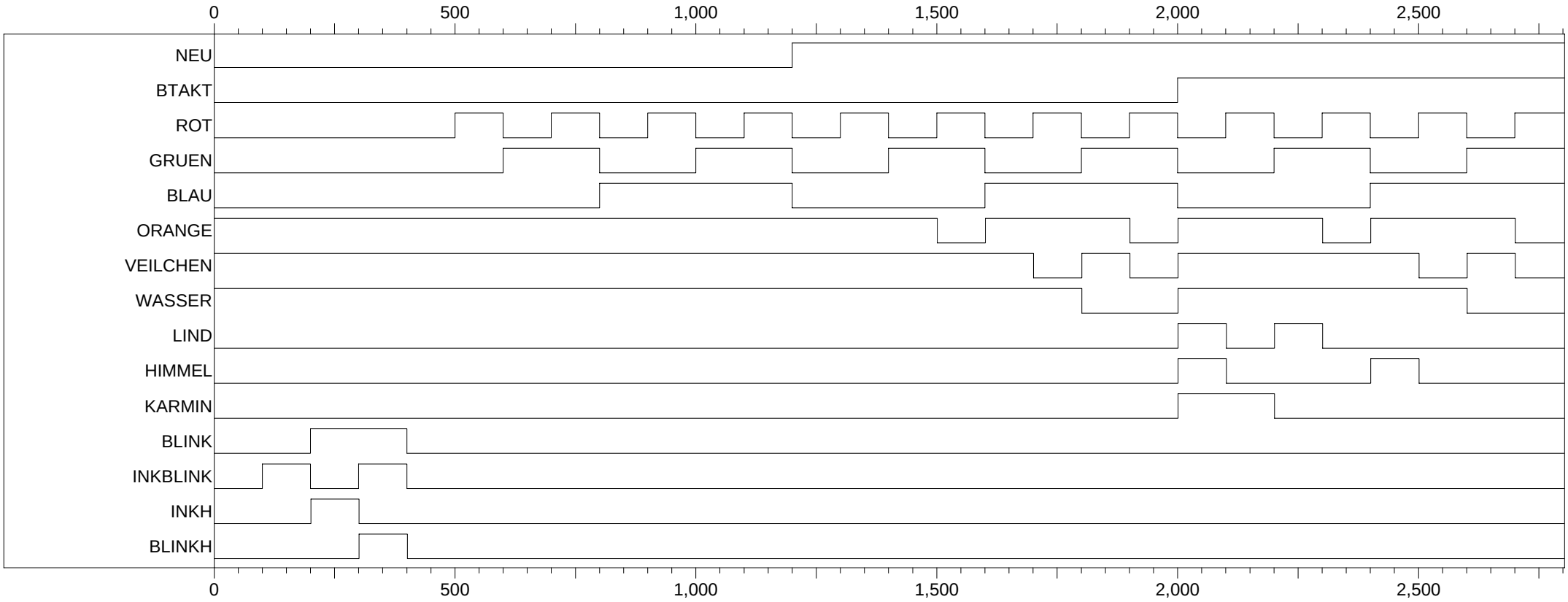

ROT
2
I_1
BLAU
3
I_2
GRUEN
4
I_3
NEU
5
I_4
BTAKT
6
I_5
BLINK
7
I_6
INKBLINK
8
I_7
I_13
I_12
I_11
I_27
I_26
I_25
I_15
I_14
19
I_24
ORANGE
18
I_23
VEILCHEN
17
I_22
WASSER
16
I_21
LIND
15
I_20
HIMMEL
14
I_19
KARMIN
13
I_18
INKH
12
I_17
BLINKH


0
500
1,000
1,500
2,000
2,500
NEU
BTAKT
ROT
GRUEN
BLAU
ORANGE
VEILCHEN
WASSER
LIND
HIMMEL
KARMIN
BLINK
INKBLINK
INKH
BLINKH
0
500
1,000
1,500
2,000
2,500

Synario 3.00 - Device Utilization Chart Thu Feb 28 18:52:11 2008

16farb.bls

Module : 'farb16'

Input files:

ABEL PLA file : farb16.tt3
Device library : P16V8AS.dev

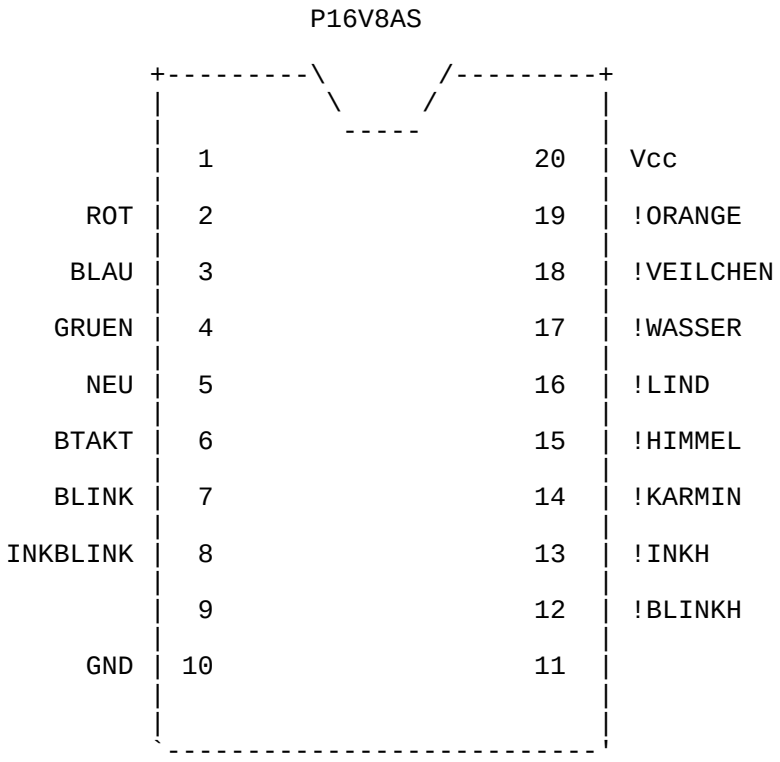
Output files:

Report file : farb16.rep
Programmer load file : farb16.jed

P16V8AS Programmed Logic:

```
BLINKH     = (  BLINK & INKBLINK );

INKH     = (  BLINK & !INKBLINK );

WASSER     = !(  BLAU & GRUEN & NEU );

VEILCHEN     = !(  ROT & BLAU & NEU );

ORANGE     = !(  ROT & GRUEN & NEU );

KARMIN     = (  !BLAU & !GRUEN & NEU & BTAKT );

HIMMEL     = (  !ROT & !GRUEN & NEU & BTAKT );

LIND     = (  !ROT & !BLAU & NEU & BTAKT );
```

P16V8AS Chip Diagram:



SIGNATURE: N/A

P16V8AS Resource Allocations:

Device Resources	Resource Available	Design Requirement	Unused
Input Pins:			
Input:	10	7	3 (30 %)
Output Pins:			
In/Out:	6	6	0 (0 %)
Output:	2	2	0 (0 %)
Buried Nodes:			
Input Reg:	-	-	-
Pin Reg:	-	-	-
Buried Reg:	-	-	-

P16V8AS Product Terms Distribution:

Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
BLINKH	12	1	8	7
INKH	13	1	8	7
WASSER	17	1	8	7
VEILCHEN	18	1	8	7
ORANGE	19	1	8	7
KARMIN	14	1	8	7
HIMMEL	15	1	8	7
LIND	16	1	8	7

==== List of Inputs/Feedbacks ====

Signal Name	Pin	Pin Type
ROT	2	INPUT
BLAU	3	INPUT
GRUEN	4	INPUT
NEU	5	INPUT
BTAKT	6	INPUT
BLINK	7	INPUT
INKBLINK	8	INPUT

P16V8AS Unused Resources:

Pin Number	Pin Type	Product Terms	Flip-flop Type
1	INPUT	-	-
9	INPUT	-	-
11	INPUT	-	-